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CORC
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,891,188 B2)
MEARS ET AL.)

Issued: May 10, 2005)

For: SEMICONDUCTOR DEVICE INCLUDING)
BAND-ENGINEERED SUPERLATTICE)

REQUEST FOR CERTIFICATE OF CORRECTION OF
APPLICANT'S MISTAKE UNDER RULE 1.323

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
OCT 26 2005
of Correction

Sir:

In accordance with the provisions of Rule 1.323 of the Rules of Practice, the Patent Office is respectfully requested to correct matters in the above-identified patent in accordance with the Certificate of Correction Form PTO-1050 attached hereto.

The Patent Office is requested to issue a Certificate of Correction on the above-referenced Patent Document, and to place such a Certificate of Correction in the file, so that such will appear on any copies of the patent which are ordered in the future.

The corrections being made are of consequence to provide the proper recitation in the drawing and specification. The mistakes occurred in good faith and are not the fault of the Patent and Trademark Office. No new matter is added by these corrections.

The Commissioner is hereby authorized to charge the requisite fee as set forth in 37 CFR § 1.20(a) in the amount of

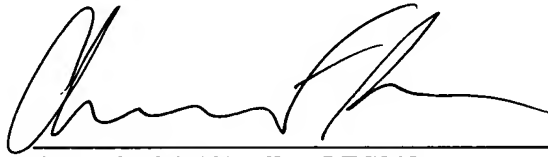
OCT 26 2005

10/24/2005 RHEBRAFT 00000010 6891188
01 FC:1811 100.00 DP

TYPE
In re Patent of
MEARS ET AL.
Patent No. 6,891,188 B2
Issued: May 10, 2005

\$100.00 to the credit card noted in the attached credit card payment form. The Commissioner is authorized to charge or credit any discrepancies in fee amounts to Deposit Account 01-0484.

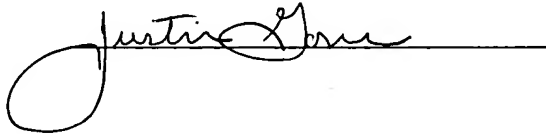
Respectfully submitted,



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& Gilchrist, P.A.
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18th day of October, 2005.



OCT 26 2005

UNITED STATES PATENT AND TRADEMARK OFFICE

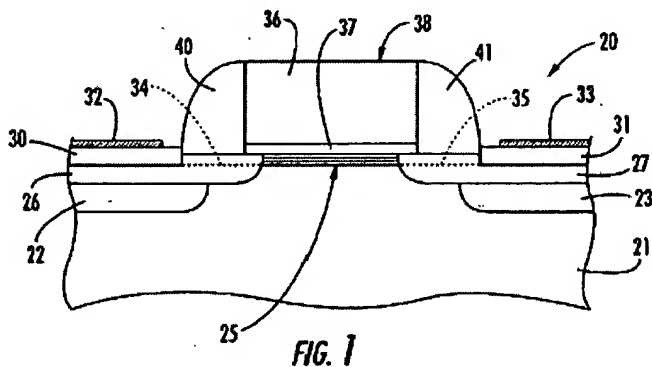
CERTIFICATE OF CORRECTION

PATENT NO.	:	6,891,188 B2
DATED	:	May 15, 2005
INVENTOR(S)	:	Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

In the Drawings

Delete: FIG. 1
Insert: New FIG. 1



Column 1, Line 42

Delete: "on a binary"
Insert: --on binary--

Column 1, Line 66

Delete: "in a silicon"
Insert: --in silicon--

Column 1, Line 67

Delete: "electromuminescence"
Insert: --electroluminescence--

MAILING ADDRESS OF SENDER:

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PATENT NO. 6,891,188 B2

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,891,188 B2
DATED : May 15, 2005
INVENTOR(S) : Mears et al.

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Column 3, Line 4	Delete: "as may" Insert: --as may be--
Column 5, Line 11	Delete: "gate 35" Insert: --gate 38--
Column 5, Line 60	Delete: "gate 35" Insert: --gate 38--
Column 7, Line 63	Delete: "from the both" Insert: --from both--
Column 9, Lines 44-46	Delete: "In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer."
Column 9, Line 59	Delete: "also formed" Insert: --also be formed--

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